ABSTRACT OF THE DISCLOSURE

Provided are a reset circuit of a data path using a clock enable signal, a reset method and a semiconductor memory device having the reset circuit. The reset circuit includes an external voltage detector and a second reset signal generator, in which the second reset signal is used to reset a block related to a data path of the semiconductor memory device. The external voltage detector detects the level of an external voltage and generates a first reset signal. The second reset signal generator performs a logical sum of an external signal, which is externally input, and the first reset signal, and generates a second reset signal. The first reset signal is used to reset blocks other than the blocks related to the data path. The external signal is a clock enable signal. In the soft reset, the blocks related to the data path are reset using the external signal which is applied at a certain level. Thus, data conflicts or ineffective data can be prevented in executing operations according to the read/write commands which are applied after the soft reset.

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